Japanese Patent Laid-Open Publication No. 56-111258

Laid-Open Date: September 2, 1981

Application No. 55-160

Application Date: January 7, 1980

Request for Examination: Not made

Inventor: Seiichi Iwamatsu

Applicant: Chou-L.S.I. Gijutsu Kenkyu Kumiai

Title of the Invention:

THIN FILM SEMICONDUCTOR DEVICE

Claims:

A thin film semiconductor device characterized in that a single crystal semiconductor film is formed over a substrate or a film made of silicon nitride through a silicon oxide film, and active regions are formed on said semiconductor film.

Detailed Description of the Invention:

This invention relates to a thin film semiconductor device fabricated by use of a single crystal semiconductor film formed over a dielectric substrate or a dielectric film.

It is known to fabricate a thin film IGFET (insulated gate field effect transistor) by the steps of forming a polycrystalline Si film over a single crystal Si substrate through a SiO_2 film, scanning (so-called "laser annealing")

the poly-Si film to convert it to a single crystal while a laser beam is irradiated to the poly-Si film to heat it, and using the Si film so converted to the single crystal.

However, such a semiconductor device is not free from the problem that ionic contaminants such as Na^+ enter the SiO_2 film as the underlying film of the single Si film and invite fluctuation of various characteristics of IGFET such as its threshold voltage V_{TH}.

It is an object of the present invention to provide a novel thin film semiconductor device that eliminates the problem described above.

The semiconductor device according to the present invention is characterized by skillfully utilizing the property of silicon nitride of impeding ionic contaminants, and by preventing the ionic contaminants from entering the SiO_2 film as the underlying film. Hereinafter, the present invention will be explained in detail with reference to an embodiment thereof shown in the accompanying drawings.

FIG. 1 shows a thin film IGFET according to an embodiment of the present invention. Reference numeral 10 denotes a single crystal Si substrate. Reference numeral 11 denotes a Si_3N_4 film formed on the substrate 10 to a thickness of 0.1 to 2 μm by a CVD process, or the like. Reference numeral 12 denotes a SiO_2 film formed on the Si_3N_4 film by the CVD process,

or the like.

The substrate 10 may be made of polycrystalline Si or a dielectric such as sapphire, quartz, or the like.

A poly-Si film or an amorphous Si film is deposited onto the SiO_2 film by the CVD process or vacuum deposition. While being irradiated and heated by a laser beam, etc, this Si film is scanned and converted to a single Si film 13. The single crystal Si film 13 is converted to a P type as a P type deciding impurity such as boron is doped before or after its crystallization to the single crystal.

A gate insulating SiO_2 film is formed on the surface of the P type Si film 13 by a thermal formation method, or the like, and a poly-Si film 15 is deposited to this SiO_2 film 14 by the CVD process, or the like. This poly-Si film 15 is patterned into a predetermined gate pattern, and the SiO_2 film 14 below the Si film 15 is then selectively etched with the Si film 15 as the mask, whenever necessary. Selective diffusion treatment or selective ion implantation treatment is carried out with Si film 15 and the SiO_2 portion below the former as the mask, forming thereby N^+ type source region 16 and drain region 17. Since an N type deciding impurity is simultaneously doped into the Si film 15, too, the Si film 15 is converted to the N^+ type (or its resistance is lowered).

In the thin film IGFET described above, the Si_3N_4 film 11 is interposed between the substrate 10 and the SiO_2 film

12 and checks invasion of the ionic contaminants into the SiO_2 film 12. Therefore, influences of the ionic contaminants on the channel region as the active region formed in the single crystal Si film 13 on the SiO_2 film can be minimized. The Si_3N_4 film 11 comes into contact with the single crystal Si film 13 not directly but through the SiO_2 film 12. Consequently, the interface charge density Q_{ss} becomes desirably small for stabilizing the characteristics. Incidentally, Q_{ss} is about $10^{12}/cm^3$ for the $Si-Si_3N_4$ interface and is about $2 \times 10^{10}/cm^3$ for the $Si-SiO_2$ interface.

FIG. 2 shows a thin film IGFET according to another embodiment of the present invention. In the drawing, like reference numerals are used to identify like constituents as in FIG. 1 and the detailed explanation of such constituents will be omitted. The feature of the device shown in FIG. 2 resides in that after holes are formed at positions corresponding to scribe lines A and B of the SiO_2 film 12 in such a way as to encompass the FET formation portion, the single crystal Si film 13 is formed, and a SiO_2 film 18 for isolation is then formed by a selective oxidation treatment in such a way as to encompass the FET formation portion. According to this arrangement, the single crystal Si film portion 13A outside the SiO_2 film 18 encompasses the FET formation portion while keeping contact with the Si_3N_4 film 11. Moreover, such an enclosure structure remains even after scribing is conducted

along the scribe lines A and B and the substrate 10 is diced into a plurality of chips or pellets. Therefore, the edge part of the SiO_2 film 12 is covered with the single crystal Si film portion 13A and is not exposed to the chip edge with the result that a greater effect of preventing ionic contamination can be obtained than in the case of FIG. 1.

FIG. 3 shows a thin film IGFET according to still another embodiment of the present invention. Like reference numerals are used in this drawing as in FIG. 1, and the explanation of like constituents will be omitted. The feature of IGFET shown in FIG. 3 is that after a ring-like hole is so formed in the SiO_2 film 12 as to encompass the FET formation portion, the FET portion is formed by the method described with reference to FIG. 1a protective film 19 of PSG (phospho-silicate glass) covers the FET portion, a ring-like hole corresponding to the ring-like hole of the SiO_2 film is then formed in the protective film 19, and the Si_3N_4 film 20 is thereafter formed over the entire surface of the substrate. According to this arrangement, the Si_3N_4 film 20 comes into contact with the Si_3N_4 film 11 on the surface of the substrate through the ring-like holes formed in the protective film 19 and in the SiO_2 film. Therefore, the FET portion is encompassed and covered as a whole with the Si_3N_4 films 11 and 20. Consequently, this embodiment provides a greater ionic contamination prevention effect and a greater passivation effect than in the cases of FIGS. 1 and

2.

Incidentally, the Si_3N_4 film is formed on the surface of the substrate in the embodiments given above but the substrate itself may well be made of a Si_3N_4 material. In such a case, the Si_3N_4 film need not be formed on the surface of the substrate.

Brief Description of the Drawings:

FIGS. 1, 2 and 3 are sectional views each showing a thin film IGFET according to a different embodiment of the present invention.

10: substrate

11: Si_3N_4 film

12: SiO_2 film

13: single crystal Si film

DIALOG(R)File 352:Derwent WPI

003216055
WPI Acc No: 1981-76612D/198142
Thin film semiconductor device - of single crystal semiconductor film formed on silicon oxide film on silicon nitride substrate
Patent Assignee: CHO LSI GIJUTSU KENKYU KUMIAI (CHOL)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 56111258	A	19810902				198142	B

Priority Applications (No Type Date): JP 80160 A 19800107
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 56111258	A		3		

Abstract (Basic): JP 56111258 A

A thin-film semiconductor device comprises a silicon nitride substrate or film, a silicon oxide formed on the silicon nitride substrate or film, a single crystal semiconductor film formed on the silicon oxide film, and active regions formed in the semiconductor film.

It is possible to prevent ionic contaminative materials from invading into a SiO2 film as an underlying layer because a Si3N4 film is formed on a substrate.

In an example a Si2N4 film and a SiO2 film are formed on a single crystal Si substrate. A polycrystalline Si film is deposited on the SiO2 film and crystallised by a laser beam to form a single crystal Si film doped with boron. A gate SiO2 film and a poly-Si gate electrode are formed on the single crystal Si film. An N+-type source and drain are formed in the single crystal Si film by ion implantation.

Title Terms: THIN; FILM; SEMICONDUCTOR; DEVICE; SINGLE; CRYSTAL; SEMICONDUCTOR; FILM; FORMING; SILICON; OXIDE; FILM; SILICON; NITRIDE; SUBSTRATE
Derwent Class: L03
International Patent Class (Additional): H01L-021/76; H01L-027/12; H01L-029/78
File Segment: CPI

00790958 **Image available**

THIN FILM SEMICONDUCTOR DEVICE

PUB. NO.: **56-111258** [JP 56111258 A]
PUBLISHED: September 02, 1981 (19810902)
INVENTOR(s): IWAMATSU SEIICHI
APPLICANT(s): CHIYOU LSI GIJUTSU KENKYU KUMIAI [470093] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-000160 [JP 80160]
FILED: January 07, 1980 (19800107)
INTL CLASS: [3] H01L-027/12; H01L-021/76; H01L-029/78
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R096 (ELECTRONIC MATERIALS -- Glass Conductors); R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS); R100 (ELECTRONIC MATERIALS -- Ion Implantation)
JOURNAL: Section: E, Section No. 84, Vol. 05, No. 186, Pg. 32, November 25, 1981 (19811125)

ABSTRACT

PURPOSE: To protect a channel region from ionic contaminated materials, by forming a monocrystalline semiconductor film with an intervention of SiO(sub 2) film on an Si(sub 3)N(sub 4) substrate or film and forming an active region thereon.

CONSTITUTION: An SiO(sub 2) film 12 is formed on an Si(sub 3)N(sub 4) film 11 which is formed on a monocrystalline Si substrate 10. A P type monocrystalline film 13 is formed on the film 12. And on the film 12, a gate insulating SiO(sub 2) film 14 and a polycrystalline Si film 15 as a gate electrode are formed, and a source region 16 and a drain region 17 are formed with the films 15, 14 as masks. In a thin film insulated gate FEt with such an arrangement, because the Si(sub 3)N(sub 4) film 11 between the substrate 10 and the film 12 prevent the intrusion of the ionic contaminated materials to the film 12, the channel region formed in the film 13 as an active region can be protected against the ionic contaminated materials.

引用文献5

⑲ 日本国特許庁（JP）　　⑪ 特許出願公開

⑫ 公開特許公報（A）　　昭56—111258

⑤Int. Cl.³	識別記号	庁内整理番号
H 01 L 27/12		6426—5F
21/76		6426—5F
29/78		6603—5F

⑬公開　昭和56年(1981)9月2日

発明の数　1
審査請求　未請求

（全 3 頁）

⑭薄膜半導体装置

⑪出　願　人　超エル・エス・アイ技術研究組合
東京都港区三田一丁目4番28号
（三田国際ビルヂング21階）
⑭代　理　人　弁理士　薄田利幸

⑪特　　願　昭55—160
⑫出　　願　昭55(1980)1月7日
⑫発　明　者　岩松誠一
川崎市高津区宮崎4丁目1番1号超エル・エス・アイ技術研究組合共同研究所内

明　細　書

発明の名称　薄膜半導体装置

特許請求の範囲

1. シリコンナイトライドからなる基板又は膜の上にシリコンオキサイド膜を介して単結晶半導体膜を形成すると共にこの半導体膜に活性領域を形成したことを特徴とする薄膜半導体装置。

発明の詳細な説明

本発明は、誘電体基板又は誘電体膜上に形成した単結晶半導体膜を用いて構成される薄膜半導体装置に関する。

従来、単結晶Si基板上にSiO_2膜を介して多結晶Si膜を形成した後、この多結晶Si膜をレーザービームで照射加熱しながら走査（いわゆるレーザーアニール）して単結晶化させ、この単結晶化されたSi膜を用いて薄膜IGFET（絶縁ゲート電界効果トランジスタ）を構成することはすでに知られている。

しかるに、このような半導体装置においては、単結晶Si膜の下地としてのSiO_2膜中にNa^+

等のイオン性汚染物質が侵入し、IGFETのスレッシュホールド電圧V_{TH}等の諸特性を変動させる不都合があつた。

本発明の目的は、このような不都合をなくした新規な薄膜半導体装置を提供することにある。

本発明による装置は、シリコンナイトライドがイオン性汚染物質を阻止する性質を有することを巧みに利用して単結晶半導体膜の下地膜としてのSiO_2膜にイオン性汚染物質が侵入するのを防止するようにしたことを特徴とするものであつて、以下、添付図面に示す実施例について詳述する。

第1図は、本発明の一実施例による薄膜IGFETを示すもので、10は単結晶Si基板、11は基板10上にCVD法等により0.1～2μmの厚さに形成されたSi_3N_4膜、12はSi_3N_4膜上にCVD法等により形成されたSiO_2膜である。基板10は多結晶Siであつてもよく、サファイア・石英等の誘電体であつてもよい。

SiO_2膜上にはCVD法又は蒸着法等により多結晶Si膜又はアモルファスSi膜が被着され、

このS1膜はレーザービーム等で照射加熱しながら走査されることにより単結晶S1膜13に変換される。単結晶S1膜13は単結晶化の前又は後の段階でボロン等のP型決定不純物をドープすることによつてP型化される。

P型S1膜13の表面には熱生成法等によりゲート絶縁用SiO_2膜14が形成され、SiO_2膜14上にはCVD法等により多結晶S1膜15が被着される。この多結晶S1膜15は所定のゲートパターンにしたがつてパターニングされ、この後必要に応じてS1膜15の下のSiO_2膜14もS1膜15をマスクとして選択エッチされる。そして、S1膜15及びその下のSiO_2部分をマスクとする選択的拡散処理又は選択的イオン打込処理によりN^+型のソース領域16及びドレイン領域17が形成され、これと同時にS1膜15にもN型決定不純物がドープされるのでS1膜15がN^+型化（低抵抗化）される。

上記した薄膜IGFETによれば、基板10とSiO_2膜12との間にSi_3N_4膜11が介在して

イオン性汚染物質のSiO_2膜12への侵入を阻止するようになつているので、SiO_2膜12上の単結晶S1膜13に形成された活性領域としてのチャンネル領域がイオン性汚染物質によつて影響されるのを最小限におさえることができる。また、単結晶S1膜13には、Si_3N_4膜11が直接でなく、SiO_2膜12を介して接するようになつているので、界面電荷密度Q_{ss}が小さくなり、特性安定化上好ましい。ちなみに、Si—Si_3N_4界面の場合のQ_{ss}は約10^{11}／cmであり、Si—SiO_2界面の場合のQ_{ss}は約2×10^{10}／cmである。

第2図は、本発明の他の実施例による薄膜IGFETを示すもので、第1図におけると同一部分には同一符号を付してその詳細な説明を省略する。第2図の装置の特徴は、SiO_2膜12のスクライブラインA，Bに対応する個所にFET形成部を取囲むように孔を形成した後、単結晶S1膜13を形成し且つFET形成部を取囲むように選択酸化処理によりアイソレーション用SiO_2膜18を

形成したことである。このようにすると、SiO_2膜18の外側の単結晶S1膜部分13AがSi_3N_4膜11と接触した形でFET形成部を取囲むようになり、しかもこのような包囲構造はスクライブラインA，Bに沿つてスクライビングを行なつて基板10を複数のチップ又はペレットに細分した後も存続する。従つて、SiO_2膜12の端縁部は単結晶S1膜部分13Aでおおわれてチップ端縁に露呈されなくなり、第1図の場合よりも一層大きなイオン性汚染防止効果を得ることができる。

第3図は、本発明の更に他の実施例による薄膜IGFETを示すもので、第1図におけると同一部分には同一符号を付してその詳細な説明を省略する。第3図の装置の特徴とするところは、SiO_2膜12にFET形成部を取囲むように環状孔を形成した後、第1図について述べたような方法によりFET部を形成し、しかる後PSG（リン・シリケート・ガラス）などからなる保護膜19に前述のSiO_2膜12に形成した環状孔に対応した環状孔を形成してから基板上に全面的にSi_3N_4

膜20を形成したことである。このようにすると、Si_3N_4膜20が保護膜19及びSiO_2膜12に形成した環状孔を介して基板表面のSi_3N_4膜11と接触するので、FET部はSi_3N_4膜11及び20で全面的に包囲被覆される。従つて、前述した第1図及び第2図の場合よりもさらに大きなイオン性汚染防止効果又はパッシベーション効果が得られるものである。

なお、上記実施例では基板表面にSi_3N_4膜を形成したが、基板そのものをSi_3N_4材で構成してもよく、この場合には基板表面にSi_3N_4膜を形成しなくてよい。

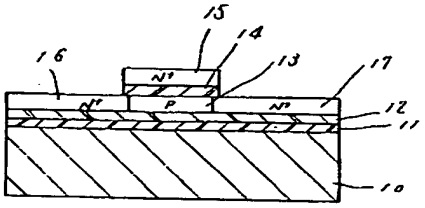
図面の簡単な説明

第1図．第2図及び第3図はそれぞれ本発明の異なる実施例による薄膜IGFETを示す断面図である。

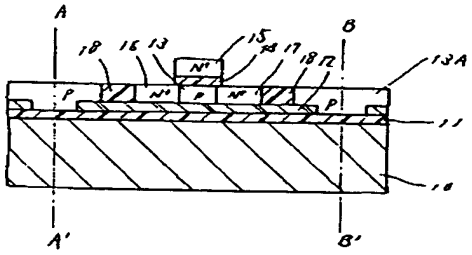
10…基板、11…Si_3N_4膜、12…SiO_2膜、13…単結晶S1膜。

代理人　弁理士　薄　田　利

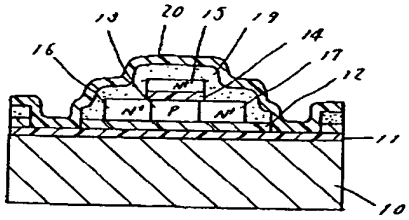
第 1 図


15
14
16
13
17
12
11
10

第 2 図


A
B
18
16
13
15
14
17
18
12
13A
11
10
A'
B'

第 3 図


13
20
15
19
14
16
17
12
11
10